REMARKS

Present Status of the Application

The Office Action rejected claims 9-17 under 35 U.S.C. 103(a), as being unpatentable over Komatsu (U.S. 6,380,053; hereafter Komatsu) in view of Liaw (U.S. 6,448,140; hereafter Liaw). Applicant respectfully traverses the rejection but has amended claims 9 and 15 to improve clarity. No new matter has been introduced into the application by the amendment made herein. After entry of the foregoing amendments, claims 9-17 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

The Office Action rejected claims 9-17 under 35 U.S.C. 103(a), as being unpatentable over Komatsu (U.S. 6,380,053) in view of Liaw (U.S. 6,448,140).

Applicant respectfully traverses this rejection and submits that Komatsu in view of Liaw is legally deficient to render claims 9 and 15 unpatentable. As stated claims 9 and 15 recite respectively:

> Claim 9. A semiconductor device, comprising:
>
> a substrate;
>
> a gate structure on said substrate, said gate structure including a gate dielectric layer on said substrate and a gate conductive layer on said gate dielectric layer;

an oxide spacer on a sidewall of said gate structure;

a spacer on said oxide spacer;

a source/drain region in said substrate besides said gate structure and said spacer; and

an offset oxide layer on said substrate and in a portion of said source/drain region, wherein **said offset oxide layer** having a bottom surface below a bottom surface of said gate dielectric layer **is separated from said gate structure by said spacer and said oxide spacer.**

Claim 15 (currently amended) A semiconductor device on a substrate, comprising:

a gate structure on the substrate;

a spacer over the sidewall of the gate structure;

a heavily doped source/drain region in a portion of the substrate exposed by the gate structure and the spacer; and

an offset oxide layer on the heavily doped source/drain region, wherein the offset oxide layer has a bottom surface below a bottom surface of the gate dielectric layer and **the offset oxide layer is separated from the gate structure by the spacer.**

(***Emphasis Added***) Applicants submit that the claims 9 and 15 patently define over the prior art of record, for at least the reason that the prior arts fail to disclose at least these elements emphasized above.

In the present invention, as shown in Fig. 1F, the semiconductor device possesses **an offset oxide layer 124 in the substrate and the offset oxide layer 124 is separated from the gate structure by the offset oxide spacer 118 and the spacer 120.**

However, Komatsu fails to teach or suggest that the silicon oxide layer (as shown in Fig. 3 of Komatsu's application) is substantially separated from the gate structure by a spacer structure. Instead, Komatsu emphasizes that the silicon oxide layer is partially transformed by oxidizing the sidewall of the polysilicon layer 21A. Komatsu further emphasizes that, for preventing channeling, the silicon oxide layer is formed on the surface of the substrate and the sidewall of the polysilicon layer after the sidewalls 22 (Fig. 2A) are removed (col. 9, lines 27-40). Because of silicon oxide layer, the thickness of the gate insulating layer 20 in the vicinity of the side wall of the gate electrode 21 can be increased and as a result, an overlap capacitance between the marginal portion of the gate electrode 21 and the source/drain region 23 can be decreased. That is, Komatsu emphasizes that the advantages of his application is achieved by oxidizing the sidewall of the polysilicon layer 21A to form the silicon oxide layer after the sidewalls 22 is removed. Apparently, the silicon oxide layer disclosed by Komatsu must be located at the substrate directly adjacent to the gate structure and partial of the silicon oxide layer is transformed from the sidewall of the polysilicon layer 21A. More specifically, the silicon oxide layer is not substantially separated from the gate structure by a spacer.

Furthermore, Komatsu never suggest or teach that the oxide layer can be formed before the sidewalls 22 (Fig. 2A) are removed. On the other words, Komatsu fails to teach or suggest that the silicon oxide layer is located on the substrate and is separated from the gate structure by a spacer. Also, no evidence can be founded in Komatsu's application to show that the sidewalls 22 still remains on the substrate adjacent to the gate structure at the time the silicon oxide layer is formed. Obviously, Komatsu's application is complete itself. Therefore, people skilled in the art would not modified Komatsu's application in view of Liaw's application by disposing the spacer on the substrate between the gate electrode and the silicon oxide layer.

Hence, even if skilled artisan modified Komatsu by referring to Liaw, the result device structure is still different from what claimed by the present invention. Additionally, in the cited art, the formation of the silicon oxide layer leads to the loss of the sidewall of the polysilicon layer 21A. That is, the polysilicon layer 21a of the gate electrode 21 is shrunk inwardly. Hence, the electrical performance of the gate electrode with the polysilicon layer 21A of which the sidewall is oxidized is quit different from that of the gate electrode of which the sidewall is covered by the spacer without being oxidized.

Hence, Applicants respectfully submit that Komatsu in view of Liaw fails to render claims 9 and 15 obvious. Claims 10-14 and 16-17, which depend from claims 9 and 15 respectively, are also patentable over Komatsu in view of Liaw, at least because of their dependency from an allowable base claim. Applicants respectfully assert that these claims are in condition for allowance. Thus, reconsideration and withdrawal of this rejection are respectively requested.

Application No.: 10/820,601 **Docket No.: JCLA12197-R**

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 9-17 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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